5 MECHANICAL SPECIFICATIONS

5.1 370-Pin SPGA Package

The pin assignments for the Cyrix III CPU in a 370-pin SPGA package are shown in Figure 5-1. Pin lists and dimensions are also included in this chapter.

Figure 5-1. Bottom View 370-Pin SPGA Package Pin Assignments

370-Pin SPGA Package

Figure 5-5. Top View 370-Pin SPGA Package Pin Assignments

Note: REVS = Reserved

Table 5-15. 370-Pin SPGA Package Signal Names Sorted by Signal Name

Signal Name	Pin	Type	I/O
A3#	AK8	GTLP	I/O
A4#	AH12	GTLP	I/O
A5#	AH8	GTLP	I/O
A6#	AN9	GTLP	I/O
A7#	AL15	GTLP	I/O
A8#	AH10	GTLP	I/O
A9#	AL9	GTLP	I/O
A10#	AH6	GTLP	I/O
A11#	AK10	GTLP	I/O
A12#	AN5	GTLP	I/O
A13#	AL7	GTLP	I/O
A14#	AK14	GTLP	I/O
A15#	AL5	GTLP	I/O
A16#	AN7	GTLP	I/O
A17#	AE1	GTLP	I/O
A18#	Z6	GTLP	I/O
A19#	AG3	GTLP	I/O
A20#	AC3	GTLP	I/O
A21#	AJ1	GTLP	I/O
A22#	AE3	GTLP	I/O
A23#	AB6	GTLP	I/O
A24#	AB4	GTLP	I/O
A25#	AF6	GTLP	I/O
A26#	Y3	GTLP	I/O
A27#	AA1	GTLP	I/O
A28#	AK6	GTLP	I/O
A29#	Z4	GTLP	I/O
A30#	AA3	GTLP	I/O
A31#	AD4	GTLP	I/O
A20M#	AE33	CMOS	I
ADS#	AN31	GTLP	I/O
BCLK	W37	GTLP	I
BNR#	AH14	GTLP	I/O
BPRI#	AN17	GTLP	I
BR0#	AN29	Ground	O
BSEL0	AJ33	CMOS/PU	I
BSEL1	AK30 AJ31	CMOS/PD	I
CPUPRES#	C37	GND	O
D0#	W1	GTLP	I/O
D1#	T4	GTLP	I/O
D2#	N1	GTLP	I/O
D3#	M6	GTLP	I/O
D4#	U1	GTLP	I/O
D5#	S3	GTLP	I/O
D6#	T6	GTLP	I/O
D7#	J1	GTLP	I/O
D8#	S1	GTLP	I/O
D9#	P6	GTLP	I/O
D10#	Q3	GTLP	I/O
D11#	M4	GTLP	I/O
D12#	Q1	GTLP	I/O
D13#	L1	GTLP	I/O
D14#	N3	GTLP	I/O
D15#	U3	GTLP	I/O
D16#	H4	GTLP	I/O
D17#	R4	GTLP	I/O
D18#	P4	GTLP	I/O
D19#	H6	GTLP	I/O
D20#	L3	GTLP	I/O
D21#	G1	GTLP	I/O
D22#	F8	GTLP	I/O
D23#	G3	GTLP	I/O
D24#	K6	GTLP	I/O
D25#	E3	GTLP	I/O
D26#	E1	GTLP	I/O
D27#	F12	GTLP	I/O
D28#	A5	GTLP	I/O
D29#	A3	GTLP	I/O
D30#	J3	GTLP	I/O
D31#	C5	GTLP	I/O
D32#	F6	GTLP	I/O
D33#	C1	GTLP	I/O
D34#	C7	GTLP	I/O
D35#	B2	GTLP	I/O
D36#	C9	GTLP	I/O
D37#	A9	GTLP	I/O
D38#	D8	GTLP	I/O
D39#	D10	GTLP	I/O
D40#	C15	GTLP	I/O
D41#	D14	GTLP	I/O
D42#	D12	GTLP	I/O
D43#	A7	GTLP	I/O
D44#	A11	GTLP	I/O
D45#	C11	GTLP	I/O
D46#	A21	GTLP	I/O
D47#	A15	GTLP	I/O
D48#	A17	GTLP	I/O
D49#	C13	GTLP	I/O
D50#	C25	GTLP	I/O
D51#	A13	GTLP	I/O
D52#	D16	GTLP	I/O
D53#	A23	GTLP	I/O
D54#	C21	GTLP	I/O
D55#	C19	GTLP	I/O
D56#	C27	GTLP	I/O
D57#	A19	GTLP	I/O
D58#	C23	GTLP	I/O
D59#	C17	GTLP	I/O
D60#	A25	GTLP	I/O
D61#	A27	GTLP	I/O
D62#	E25	GTLP	I/O
D63#	F16	GTLP	I/O
DBSY#	AL27	GTLP	I/O
DEFER#	AN19	GTLP	I/O
DRDY#	AN27	GTLP	I/O
EXTRATIO#	AB2	CMOS/PD	O
FERR#	AC35	CMOS	O
FLUSH#	AE37	CMOS	I
HIT#	AL25	GTLP	I/O
HITM#	AL23	GTLP	I/O
IERR#	AE35	Pull Up	O
IGNNE#	AG37	CMOS	I
INIT#	AG33	CMOS	I
INTR	M36	CMOS	I
LOCK#	AK20	GTLP	I/O
NMI	L37	CMOS	I
PLL_GND	U33	VSSPLL	
PLL_VDD	W33	VDDPLL	
PWRGOOD	AK26	CMOS	I
REQ0#	AK18	GTLP	I/O
REQ1#	AH16	GTLP	I/O
REQ2#	AH18	GTLP	I/O
REQ3#	AL19	GTLP	I/O
REQ4#	AL17	GTLP	I/O
RESET#	X4	GTLP	I
RS0#	AH26	GTLP	I/O
RS1#	AH22	GTLP	I/O
RS2#	AK28	GTLP	I/O
SLP#	AH30	CMOS	I
SMI#	AJ35	CMOS	I
STPCLK#	AG35	CMOS	I
TCLK	AL33	CMOS/PU	I
TDI	AN35	CMOS/PU	I
TDO	AN37	CMOS	O
THERMDN	AL29	ESD only	O
THERMDP	AL31	ESD only	O
THRMTRIP#	AH28	CMOS/PU	I/O
TMS	AK32	CMOS/PU	I
TRDY#	AN25	GTLP	I/O
TRST#	AN33	CMOS/PU	I
VID0	AL35	Voltage ID	O
VID1	AM36	Voltage ID	O
VID2	AL37	Voltage ID	O

Table 5-2. 370-Pin SPGA Package Signal Names Sorted by Pin Number

Package Pin	Signal Name	Pad Type	I/O
A3	D29#	GTLP	I/O
A5	D28#	GTLP	I/O
A7	D43#	GTLP	I/O
A9	D37#	GTLP	I/O
A11	D44#	GTLP	I/O
A13	D51#	GTLP	I/O
A15	D47#	GTLP	I/O
A17	D48#	GTLP	I/O
A19	D57#	GTLP	I/O
A21	D46#	GTLP	I/O
A23	D53#	GTLP	I/O
A25	D60#	GTLP	I/O
A27	D61#	GTLP	I/O
B2	D35#	GTLP	I/O
C1	D33#	GTLP	I/O
C5	D31#	GTLP	I/O
C7	D34#	GTLP	I/O
C9	D36#	GTLP	I/O
C11	D45#	GTLP	I/O
C13	D49#	GTLP	I/O
C15	D40#	GTLP	I/O
C17	D59#	GTLP	I/O
C19	D55#	GTLP	I/O
C21	D54#	GTLP	I/O
C23	D58#	GTLP	I/O
C25	D50#	GTLP	I/O
C27	D56#	GTLP	I/O
C37	CPUPRES#	GND	O
D8	D38#	GTLP	I/O
D10	D39#	GTLP	I/O
D12	D42#	GTLP	I/O
D14	D41#	GTLP	I/O
D16	D52#	GTLP	I/O
E1	D26#	GTLP	I/O
E3	D25#	GTLP	I/O
E25	D62#	GTLP	I/O
F6	D32#	GTLP	I/O
F8	D22#	GTLP	I/O
F12	D27#	GTLP	I/O
F16	D63#	GTLP	I/O
G1	D21#	GTLP	I/O
G3	D23#	GTLP	I/O
H4	D16#	GTLP	I/O
H6	D19#	GTLP	I/O
J1	D7#	GTLP	I/O
J3	D30#	GTLP	I/O
K6	D24#	GTLP	I/O
L1	D13#	GTLP	I/O
L3	D20#	GTLP	I/O
L37	NMI	CMOS	I
M4	D11#	GTLP	I/O
M6	D3#	GTLP	I/O
M36	INTR	CMOS	I
N1	D2#	GTLP	I/O
N3	D14#	GTLP	I/O
P4	D18#	GTLP	I/O
P6	D9#	GTLP	I/O
Q1	D12#	GTLP	I/O
Q3	D10#	GTLP	I/O
R4	D17#	GTLP	I/O
S1	D8#	GTLP	I/O
S3	D5#	GTLP	I/O
T4	D1#	GTLP	I/O
T6	D6#	GTLP	I/O
U1	D4#	GTLP	I/O
U3	D15#	GTLP	I/O
U33	PLL_GND	VSSPLL	
W1	D0#	GTLP	I/O
W33	PLL_VDD	VDDPLL	
W37	BCLK	GTLP	I
X4	RESET#	GTLP	I
Y3	A26#	GTLP	I/O
Z4	A29#	GTLP	I/O
Z6	A18#	GTLP	I/O
AA1	A27#	GTLP	I/O
AA3	A30#	GTLP	I/O
AB2	EXTRATIO#	CMOS/PD	O
AB4	A24#	GTLP	I/O
AB6	A23#	GTLP	I/O
AC3	A20#	GTLP	I/O
AC35	FERR#	CMOS	O
AD4	A31#	GTLP	I/O
AE1	A17#	GTLP	I/O
AE3	A22#	GTLP	I/O
AE33	A20M#	CMOS	I
AE35	IERR#	Pull Up	O
AE37	FLUSH#	CMOS	I
AF6	A25#	GTLP	I/O
AG3	A19#	GTLP	I/O
AG33	INIT#	CMOS	I
AG35	STPCLK#	CMOS	I
AG37	IGNNE#	CMOS	I
AH10	A8#	GTLP	I/O
AH12	A4#	GTLP	I/O
AH14	BNR#	GTLP	I/O
AH16	REQ1#	GTLP	I/O
AH18	REQ2#	GTLP	I/O
AH22	RS1#	GTLP	I/O
AH26	RS0#	GTLP	I/O
AH28	THRMTRIP#	CMOS/PU	I/O
AH30	SLP#	CMOS	I
AH6	A10#	GTLP	I/O
AH8	A5#	GTLP	I/O
AJ1	A21#	GTLP	I/O
AJ31	BSEL1	CMOS/PD	
AJ33	BSEL0	CMOS/PU	I
AJ35	SMI#	CMOS	I
AJ37	VID3	Voltage ID	O
AK6	A28#	GTLP	I/O
AK8	A3#	GTLP	I/O
AK10	A11#	GTLP	I/O
AK14	A14#	GTLP	I/O
AK18	REQ0#	GTLP	I/O
AK20	LOCK#	GTLP	I/O
AK26	PWRGOOD	CMOS	I
AK28	RS2#	GTLP	I/O
AK30	BSEL1	CMOS/PD	I
AK32	TMS	CMOS/PU	I
AK36	VID4	Voltage ID	O
AL5	A15#	GTLP	I/O
AL7	A13#	GTLP	I/O
AL9	A9#	GTLP	I/O
AL15	A7#	GTLP	I/O
AL17	REQ4#	GTLP	I/O
AL19	REQ3#	GTLP	I/O
AL23	HITM#	GTLP	I/O
AL25	HIT#	GTLP	I/O
AL27	DBSY#	GTLP	I/O
AL29	THERMDN	ESD only	O
AL31	THERMDP	ESD only	O
AL33	TCLK	CMOS/PU	I
AL35	VID0	Voltage ID	O
AL37	VID2	Voltage ID	O
AM36	VID1	Voltage ID	O
AN5	A12#	GTLP	I/O
AN7	A16#	GTLP	I/O
AN9	A6#	GTLP	I/O
AN17	BPRI#	GTLP	I
AN19	DEFER#	GTLP	I/O
AN25	TRDY#	GTLP	I/O
AN27	DRDY#	GTLP	I/O

Table 5-15. Voltage and Reserved Pins

VOLTAGE LEVEL	PURPOSE	PINS
VCC	Voltage Inputs. Supplies nominal 2.2 volts to processor core.	B6, B10, B14, B18, B22, B26, B30, B34, C3, D6, D20, D24, D28, D32, D36, E5, E9, E13, E17, H32, F2, F4, F14, F22, F26, F30, F34, H36, J5, K2, K32, K34, M32, N5, P2, P34, R32, R36, S5, T2, T34, V32, V36, W5, X34, Y35, Z32, AA5, AA37, AB2, AB34, AD32, AE5, AF2, AF34, AH24, AH32, AH36, AJ5, AJ9, AJ13, AJ17, AJ21, AJ25, AJ29, AK2, AK34, AM12, AM4, AM8, AM16, AM20, AM24, AM28, AM32
VCC_1.5V	Voltage Input. Supplies 1.5 volts to processor core	AD36
VCC_2.5V	Voltage Input. Supplies 2.5 volts to processor I/O	Z36
VCC_CMOS	Voltage Output. Connects to VCC_2.5. Supplies 2.5 volts to motherboard or other component.	AB36
VREF[0-7]	Voltage Input. Establishes reference voltage for GTL+ logic switching level.	V_{REF0} E33 V_{REF1} F18 V_{REF2} K4 V_{REF3} R6 V_{REF4} V6 V_{REF5} AD6 V_{REF6} AK12 V_{REF7} AK22
GND	Return path for all voltages.	A37, B4, B8, B12, B16, B20, B24, B28, B32, D2, D4, D18, D22, D26, D30, D34, E7, E11, E15, E19, F20, F24, F28, F32, F36, G5, H2, H34, K36, L5, M2, M34, P32, P36, Q5, R34, T32, T36, U5, V2, V34, X36, Y5, Y33, Y37, X32, Z2, Z34, AB32, AC33, AC5, AD2, AD34, AF32, AF36, AG5, AH2, AH34, AJ3, AJ7, AJ11, AJ15, AJ19, AJ23, AJ27, AJ31, AK4, AL1, AL3, AM6, AM10, AM14, AM18, AM2, AM22, AM26, AM30, AM34, AN3
Reserved Pins	These pins are used for factory testing or reserved for future use. Generally compatible with Celeron™ processor defined pins.	A29, A31, A33, A35, B36, C29, C31, C33, C35, E21, E23, E27, E29, E31, E35, E37, F10, G33, G35, G37, J33, J37, J35, L33, L35, N33, N35, N37, Q33, Q35, Q37, R2, S33, S35, S37, U35, U37, V4, W3, W35, X2, X6, Y1, AA33, AA35, AC1, AC37, AF4, AG1, AH4, AH20, AK16, AK24, AL11, AL13, AL21, AN11, AN13, AN15, AN21, AN23, AN29

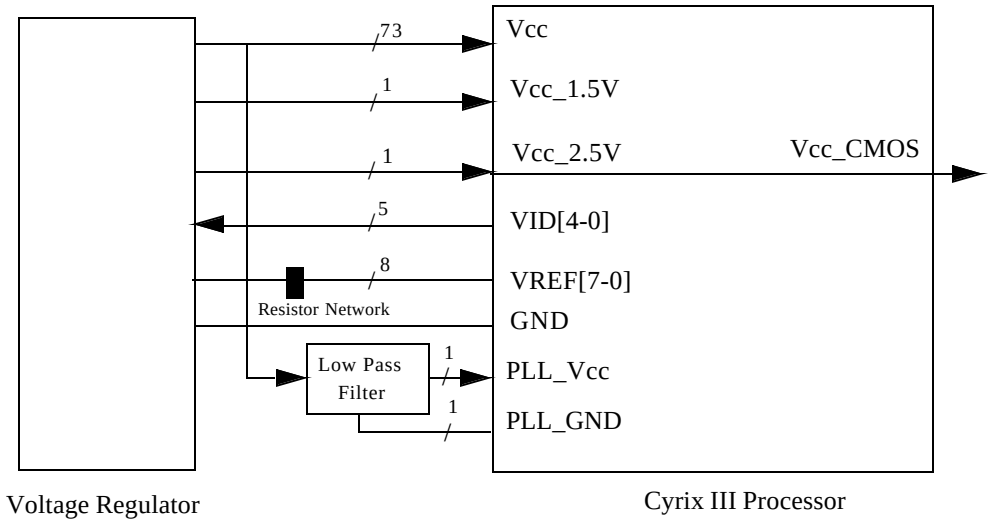

Figure 5-3. Typical Connections Between Voltage Regulator and Cyrix III Processor

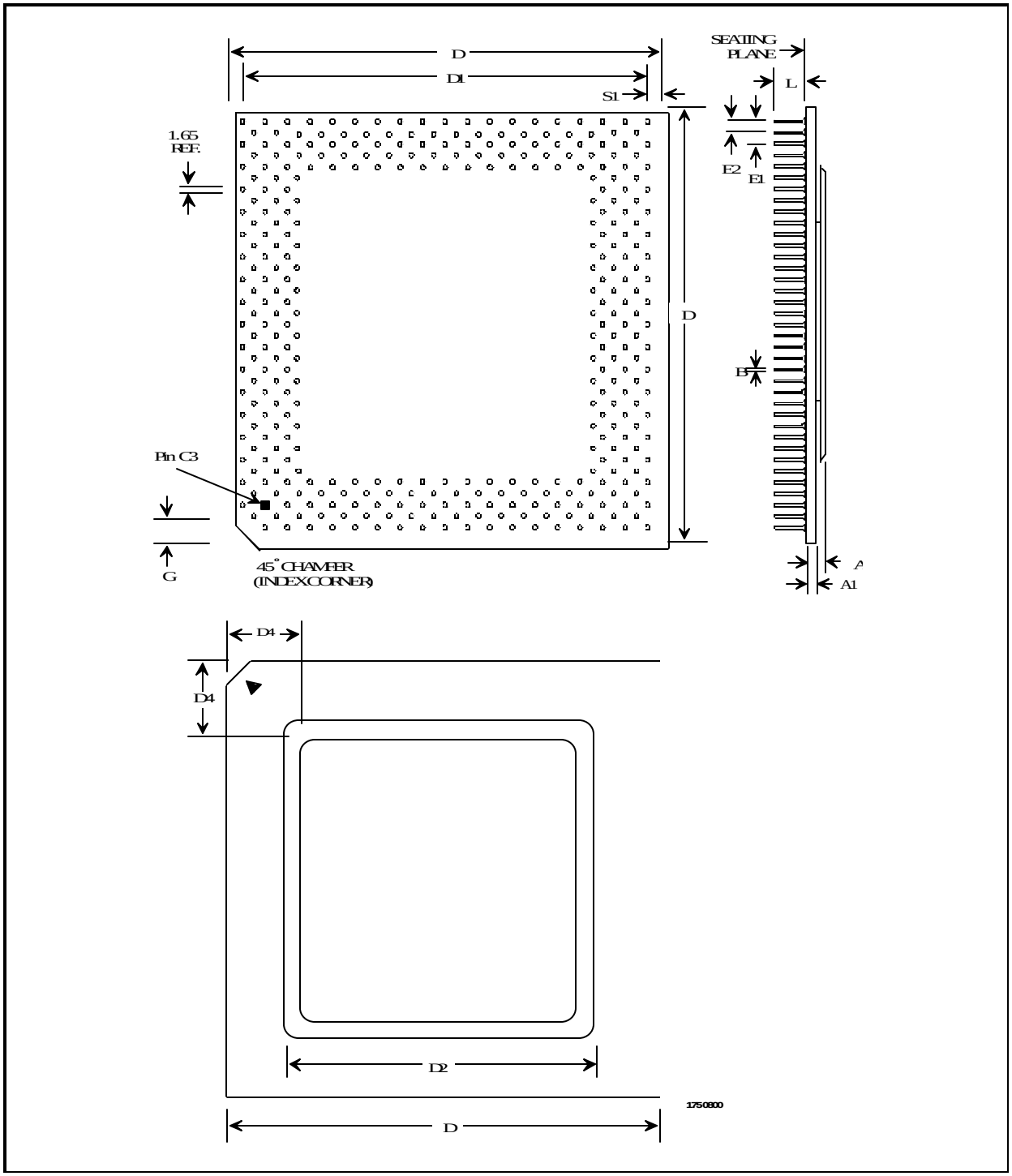

Figure 5-4. 370-Pin “Flip Chip SPGA

Table 5-16. 370-Pin SPGA Dimensions

SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	3.80	4.50	0.150	0.177
A1	1.62	1.98	0.064	0.078
B	0.43	0.51	0.017	0.020
D	49.28	49.91	1.940	1.965
D1	45.47	45.97	1.790	1.810
D2	36.75 Sq.	37.25 Sq.	1.447	1.467
E1	2.41	2.67	0.095	0.105
E2	1.14	1.40	0.045	0.055
G	1.52	2.29	0.060	0.090
L	2.97	3.38	0.117	0.133
S1	1.65	2.16	0.065	0.085

5.2 Thermal Resistances

Three thermal resistances can be used to idealize the heat flow from the junction of the Cyrix III CPU to ambient:

θ_{JC} = thermal resistance from junction to case in °C/W

θ_{CS} = thermal resistance from case to heatsink in °C/W,

θ_{SA} = thermal resistance from heatsink to ambient in °C/W,

$\theta_{CA} = \theta_{CS} + \theta_{SA}$, thermal resistance from case to ambient in °C/W.

$T_C = T_A + P * \theta_{CA}$ (where T_A = ambient temperature and P = power applied to the CPU).

To maintain the case temperature under 85°C during operation θ_{CA} can be reduced by a heat-sink/fan combination. (The heatsink/fan decreases θ_{CA} by a factor of three compared to using a heatsink alone.) The required θ_{CA} to maintain 85°C is shown in Table 5-4. The designer should ensure that adequate air flow is maintained to control the ambient temperature (T_A). A typical θ_{JC} value for the Cyrix III 370-pin PGA-package value is 0.5 °C/W.

Cyrix III Performance Rating	Cyrix III Actual MHz	Max Active Current (A)	Max Active Power (W)	Θ_{CA} For Different Ambient Temperatures				
				25°C	30°C	35°C	40°C	45°C
PR 433	333 MHz	9.15	20.1	2.98	2.74	2.50	2.24	1.99
PR 466	366 MHz	9.76	21.5	2.79	2.55	2.33	2.09	1.86
PR 500	400 MHz	10.40	22.9	2.62	2.40	2.18	1.96	1.75
PR 533	433 MHz	10.85	23.9	2.51	2.30	2.09	1.88	1.67
PR 533	450 MHz	11.20	24.6	2.41	2.24	2.03	1.83	1.63

Required θ_{CA} to Maintain 85°C Case Temperature

Thermal Resistances